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| 10/686,270 | 10/16/2003 | Yong-Hyun Lee | 45533 | 7218 |

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| EXAMINER | |
|---|---|
| BORKOWSKI, ROBERT | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/686,270 | LEE, YONG-HYUN | |
| | Examiner | Art Unit | |
| | Robert Borkowski | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of Claims*

Claims 1-21 stand rejected.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-5, 8-12, 15-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Landi et al. (U.S. Patent No. 6,163,828) in view of Silverbrook (U.S. Patent No. 5,430,496).

**As per claims 1, 8, and 15**, Landi et al. teaches a memory control apparatus (column 3 lines 14-16, fig. 2 element 100), adapted to operate with a plurality of digital signal processors (CPU and DSP) (column 3 lines 14-21, Fig. 2 elements 105, 110), the memory control apparatus comprising:

a switch (Fig. 2 elements 170+172+174+176+178), adapted to selectively route signals for input to the DSPs from a memory (Fig. 2 elements 115) and for output from the DSPs to the memory (column 3 lines 45-52);

a controller (Fig. 2 element 120), adapted to control the switch (170+172+174+176+178) to route the signals to and from the memory and DSPs (column 3 lines 26-29, 55-58) and to control the buffer (174+178) to selectively output the memory information (column 3 lines 36-44, Fig. 2, elements 120).

Although Landi et al. teaches a buffer (250+260+255+265+270, and 250+260+255+265), Landi et al. is silent regarding a buffer coupled to an insert terminal of the memory and of each DSP, the buffer being adapted to receive memory information comprising an insert signal from the memory and output the insert signal to the insert terminal of each DSP to selectively output to the DSPs information indicating that the memory is available. However, Silverbrook teaches a buffer (see Silverbrook Fig. 1A element 13) coupled to an insert terminal (Fig. 1A element 10) of the memory (Fig. 1A element 17) and of each DSP (Fig. 1A elements 5 and 15), the buffer being adapted to receive memory information comprising an insert signal from the memory and output the insert signal to the insert terminal of each DSP to selectively output to the DSPs information indicating that the memory is available (see Silverbrook column 4 lines 8-44, Fig. 1A).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quiet advantageous for the apparatus of Landi et al. use a buffer coupled to an insert terminal and the memory and each of the of DSP in order to ensure that the memory card does not directly interfere with the logic level of the processor bus at any stage (see Silverbrook column 4 lines 8-31).

It is for this reason that one of ordinary skill in the art be motivated to implement Landi et al. apparatus with a buffer coupled to an insert terminal and the memory and each of the of DSP in order to ensure that the memory card does not directly interfere with the logic level of the processor bus at any stage.

**As per claims 2-3, 9-10, 16-17** Landi et al. is silent wherein the memory is a removable memory, and the memory information indicates that the memory has been inserted into a port for access by the memory control apparatus. However, Silverbrook teaches wherein the memory is a removable memory (see Silverbrook Fig. 1A element 17), and the memory information indicates that the memory has been inserted into a port (see Silverbrook Fig. 1A element 10) for access by the memory control apparatus (see Silverbrook column 4 lines 8-44).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quiet advantageous for the apparatus of Landi et al. use a removable memory in order to storage of user's data and accommodate memory cards with increased storage capabilities as they become available (see Silverbrook column 4 lines 3-7).

It is for this reason that one of ordinary skill in the art be motivated to implement Landi et al. apparatus with a removable memory in order to storage of user's data and accommodate memory cards with increased storage capabilities as they become available (see Silverbrook column 4 lines 3-7).

**As per claims 4, 11, and 18**, Landi et al. teaches the switch includes a plurality of selection switches, coupled between the DSPs and the memory, which are controlled by the controller (column 3 lines 55-58, Fig. 2 elements 130, 140, 150, 170, and 180).

**As per claims 5, 12, and 19**, Landi et al. teaches the buffer includes a three-state buffer which selectively outputs the memory information of the memory to the DSPs as controlled by the controller (column 3 lines 61-65, Fig. 2 elements 182, 174, 178).

2. **Claims 6-7, 13-14, and 20-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Landi et al. (U.S. Patent No. 6,163,828) and Silverbrook (U.S. Patent No. 5,430,496) as applied to claims 1,8,15 above, and further in view of Ono (U.S. Patent Application No. 2003/0020814).

**As per claims 6, 13, and 20** the teaching of Landi et al. as modified by the teaching of Silverbrook as applied above, teach a memory control apparatus adapted to operate with a buffer coupled to an insert terminal and the memory and each of the of DSP (see Silverbrook column 4 lines 8-31). However, Landi et al. and Silverbrook fail to teach a key input unit, adapted to indicate an operation mode; and wherein the control unit controls recording of data in the memory or reproduction of data from the memory according to the operation mode indicated by the key input unit.

Ono discloses an operation unit (Fig. 2 element 110) containing a function setting portion (Fig. 2 element 116). Depending on the status of the function settings option (Fig.2 element 116) the digital camera (Fig. 1 element 10) is in a capture or a playback mode (paragraph 0074 lines 1-4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Landi et al. and Silverbrook to include the function setting portion (see Ono Fig. 2 element 116) of the operation unit (Fig.2 element 110) to control recording of data in the memory (see Ono paragraph 0076-0077) or reproduction of data from the memory (see Ono paragraph 0078) according to the operation mode indicated by the status of the function setting portion (see Ono Fig. 2 element 116). The function setting portion (see Ono Fig. 2 element 116) of the operation unit (see Ono Fig. 2 element 110) allows the user to specify (see Ono paragraph 0045) operation mode by selecting the memory operation mode. Using the function setting portion (see Ono Fig. 2 element 116) the user is able to switch and control the operation mode to either a capture mode or a playback mode (see Ono paragraph 0074). The user does not have to perform any additional or complicated steps to change between capture and playback modes because the function setting portion (see Ono Fig. 2 element 116) is constantly monitored by the internal circuitry (see Ono paragraph 0074 lines 1-4). Once the user selects (see Ono paragraph 0045) the desired mode of operation through the function setting portion (see Ono Fig. 2 element 116) the selected operation mode will be performed.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Landi et al. and Silverbrook by teaching of Ono, because including the function setting portion (see Ono Fig. 2 element 116) would allow the user to select the operation mode at a glance and it would allow the user to

select an operation mode to either record data in the memory or reproduce data from the memory without any additional or complex steps.

**As per claims 7, 14, and 21** the teaching of Landi et al. as modified by the teaching of Silverbrook as applied above, teach a memory control apparatus adapted to operate with a buffer coupled to an insert terminal and the memory and each of the of DSP (see Silverbrook column 4 lines 8-31). However, Landi et al. and Silverbrook fail to teach that one of the DSPs is employed with a digital still camera and another of the DSPs is employed with a digital video camera.

Ono discloses two separate capture signal processors (Fig. 10 elements 32a and 32b) that perform different types of image processing for the corresponding capture signal output from the respective CCDs depending on the types of the capturing optical systems (paragraph 0097, Fig. 10 elements 21a and 21b).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Landi et al. and Silverbrook wherein the first capture signal processor (see Ono Fig. 10 element 32a) performs predetermined image processing for the first capture optical system (see Ono Fig. 10 element 21a) and the second capture signal processor (see Ono Fig. 10 element 32b) performs predetermined image processing for the second capture optical system (see Ono Fig. 10 element 21b). The capturing optical systems (Fig. 10 elements 21a and 21b) are different from each other (see Ono paragraph 0062). The first image capturing optical system (see Ono Fig. 10 element 21a) is used for capturing still images and the second image capturing optical system (see Ono Fig. 10 element 21b) may be used as

a video movie camera for capturing movies (see Ono paragraphs 0099 and 0103). Because digital still cameras and digital video cameras might differ from each other, thus still image camera might require a specialized signal processor to perform a specific set of operations where the specific set of operations of the still camera's signal processor might not be sufficient to perform video camera's operations. Thus, employing individual capture signal processor (see Ono Fig. 10 elements 32a and 32b) capable of performing the optimal image processing with a single capturing optical system (see Ono Fig. 20 element 21a and 21b) increases the freedom of design and it allows to use the specialized signal processor with the optimal performance for the task of processing signals from the specific capturing optical system (see Ono paragraph 0099).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Landi et al. and Silverbrook by teaching of Ono, because employing a separate signal processor (see Ono Fig. 10 element 32a) with a single capturing optical system (see Ono Fig. 10 element 21a) for still image capture and employing a separate signal processor (see Ono Fig. 10 element 32b) with a single capturing optical system (see Ono Fig. 10 element 21b) for video capture, would allow to use the optimal signal processor for the tasks the processor was designed for.

***Response to Amendment***

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.13(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Borkowski whose telephone number is 571-272-8626. The examiner can normally be reached on Monday - Friday 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM NGOC (KIM) HUYNH can be reached on 571-272-4147. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert Borkowski
Art unit 2181
1/31/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/2/06